ACTIVE PIXEL SENSOR

~~APS and HIT abstracts for the NGST Detector~~ Workshop

V. PAIN AND G. DOMINGO

APS Abstract

The Active Pixel Sensor (APS) is a fully integrated NIR/Visible imager fabricated using standard or radiation hard CMOS processes. The APS contains the visible array (either photogate or photodiode), all the control electronics and DAC's needed to operate the array and the ADCs to read the signal digitally. The APS is truly a Digital Camera-on-a-Chip (DCC). It operates with four inputs (DC, ground, master clock and serial instruction) and one (or two) digital outputs. These miniature self-contained cameras will be used for navigation, start tracking and scientific missions.

JPL has successfully demonstrated a 512 x 512, 12 μm^2 unit cell APS with 40 to 60% QE, less than 20 e-, 250 Ke- full well, a 10 bit ADC, with a power dissipation under 10 mW at full video rates. At this time, JPL is developing a 1K x 1K APS and a 512 x 512 Radiation Hard APS. In addition to the digital output, JPL is demonstrating on chip signal processing such as multiwindowing, offset correction, CDS and cetroid.

This poster will display the goals of the program, the performance achieved at this time with existing devices and the plans for future work.

HIT Abstract

The Hybrid Imaging Technology (HIT) is an integrated visible/NIR imager merging, through indium bump hybridization, the highly successful CCD technology for the imaging portion of the array, with CMOS electronics for the drive electronic and to digitize and read-out the digital output. This hybrid approach combines the high QE, 100% fill factor and the low noise of the CCD technology with the low power, radiation hardness and supporting electronics of the CMOS technology. The hybrid approach provides the flexibility to select the best and most appropriate electronic processes and designs for any given imaging application.

JPL has built and tested the first prototype, a 256 x 512 array achieving a QE of xxx%, a noise under 5e- and a linearity of 99.5% at a 50 Kilopixels/sec rate. This performance has been achieved with the array operating under 100 μWatts. JPL is now developing a 1K x 1K array with CMOS variable gain amplifiers, CDS, ADC and digital logic for timing generation and drivers. A similar array is being designed and will be fabricated in a radiation hard foundry.

The HIT poster will display the goals of the program, the performance achieved to date and the plans for future work.